PCI-SIG ENGINEERING CHANGE REQUEST

TITLE:	M.2 8GT/s Compliance ECR
DATE:	December 08, 2018
AFFECTED DOCUMENT:	PCIe M.2 Specification_Rev1.1
SPONSOR:	Intel

Part I

1.1. Summary of the Functional Changes

This proposal introduces 8GT/s electrical compliance details for M.2 based SSDs.

1.2. Benefits as a Result of the Changes

Currently there is no defined compliance program or methodology to test M.2 Add-in Cards or M.2 based Platforms supporting PCIe interface.

Some companies use CEM to M.2 adapter for doing this testing, which gives pessimistic results due to additional connector present during the testing.

This ECR defines the transmitter and receiver compliance requirements to test M.2 Add-in Card and M.2 Socket on a platform. This compliance requirement is being added for Socket-3 and Key-M that supports Storage based applications.

Other Sockets and Keys may use this as a guideline.

1.3. Assessment of the Impact

This change enables the PCI-SIG Serial Enabling WG to start the compliance program and Integrators list for M.2 Socket-3 and Key-M based devices.

1.4. Analysis of the Hardware Implications

None.

1.5. Analysis of the Software Implications

None.

1.6. Analysis of the C&I Test Implications

This change enables the PCI-SIG Serial Enabling WG to start the compliance program for M.2 Socket 3 and Key-M based devices. Adding the Transmitter and Receiver Eye and jitter limits enables the SEG to develop the compliance test procedures and make any updates to the test specifications, if needed.

It is determined that for testing M.2 8GT/s devices, same compliance eye limits as CEM 3.0 can be used. The s-parameters that are embedded using the post-processing tool are different than CEM 3.0 due to differences in the Max length supported on the Add-in Card PCB routing and the device package.

1.6.1. Changes to M.2 v1.1

[Editor's note: Existing M.2 v1.1 text is black. New text is marked in blue. Material to be deleted ~~is red with strikethrough~~.]

Add following sections to the M.2 Specification Rev 1.1:

Add reference to *PCIe Architecture PHY test specification Rev 3.0* in the specification references section.

x.y. Compliance Eye Limits at the M.2 Connector

The compliance eye limits defined in this section must be met for both M.2 Key-M Add-in Card and a Platform interfacing with such an Add-in Card. The specific measurement requirements (probe test points, calibrated system board specifics, etc.) for compliance of physical components are to be specified in the PCI Express Architecture, PHY Test Specification document. A minimum sample size of 1.5×10^6 UI is required at 8.0GT/s.

x.y.1 Add-in Card Transmitter Path Compliance Eye Diagrams at 8.0 GT/s

Eye Height (V_{TXA}, V_{TXA_d}) and Eye Width (T_{TXA}) limits for the M.2 Key-M based Add-in Card's Transmitter path compliance at 8GT/s are defined in Table a-b.

The Add-in Card shall pass the eye diagram requirements with at least one of the transmitter equalization presets defined in the *PCI Express Base Specification*, Chapter 9. The eye diagram requirements are evaluated after the behavioral CDR and the behavioral receiver Equalization Algorithm defined in the *PCI Express Base Specification*, Chapter 9 are applied.

A worst-case reference clock with 1 ps RMS jitter is assumed for this revision of the specification. All Links are assumed active while generating this eye diagram. The eye diagram requires that the compliance pattern in 128b/130b (refer to the PCI Express Base Specification, Chapter 4) is being transmitted during the test. Transition and non-transition bits must be distinguished to measure compliance against the de- emphasized voltage level (V_{TXA_d}). V_{TXA} and V_{TXA_d} are minimum differential peak-peak output voltages.

The calculated eye width at BER 10^{-12} must be greater than or equal to T_{TXA}.

The values in Table a-b are referenced to an ideal 100 Ω differential load at the end of an isolated (no crosstalk) test channel consisting of approximately three inches of 85 ohm trace followed by 12.1dB of 85 Ω trace, all behind a standard M.2 connector. This channel shall be referenced as the 8.0 GT/s M.2 Add-in Card Test Channel. This channel is same as the CEM 3.0 Add-in Card Test Channel, but has additional 2" trace added to the Motherboard side to account for the differences in worse case CEM 3.0 Add-in Card routing (4") and M.2 Add-in Card routing (2"). S-parameters for the channel are provided with the specification. Additional loss from the measurement set-up must be removed. The Add-in Card Test Channel is a reference channel for testing and does not represent the worst possible channel that could be implemented on a M.2 compliant motherboard.

Table a-b. M.2 Key-M based Add-in Card Transmitter Path Compliance Eye Limits at 8 GT/s

Parameter	Min	Max	Unit	Comments
V_{TXA}	34 (at 10^{-12} BER) 46 (at 10^{-6} BER)	1300	mV	
V_{TXA_d}	34 (at 10^{-12} BER) 46 (at 10^{-6} BER)	1300	mV	
T_{TXA}	41.25 (at 10^{-12} BER)		ps	Notes 1

Notes:

1. T_{TXA} is the minimum eye width. The recommended sample size for this measurement is at least $1.5x10^6$ UI.

x.y.2 Add-in Card Minimum Receiver Path Sensitivity Requirements at 8.0 GT/s

The minimum sensitivity values for the Add-in Card's Receiver path compliance at 8.0 GT/s are defined in Table c-d. The receiver path shall be tested with a worst-case eye to verify that it achieves a BER < 10^{-12}. This worst-case eye is calibrated using transmitter equalization settings that are optimal with the reference equalizer for each calibration channel. After calibration, the test-generator's transmitter equalization may be adjusted using the setting in the required transmitter equalization space preferred by the device under test, without changing any other parameter of the test signal or recalibrating the test signal.

If the test generator's transmitter equalization settings are adjusted away from the optimal settings and the test generator is not able to change transmitter equalization without impacting other calibrated parameters –then the other parameters must be adjusted back to the specified values.

If the test is not run in a way that produces the worst-case cross-talk that would be present with all lanes active, the additional cross-talk must be accounted for in some other way. The test is performed with two different test channels, a long test channel and a short test channel. While the receiver's capacity to adapt its own equalization is part of the test, its ability to request the link partner's transmitter to change its transmitter equalization is tested by applying a signal whose equalization level is suboptimal compared to the jitter sensitivity test signal described above. For this signal, the reference receiver would not be able to achieve proper equalization by means of its own CTLE and DFE alone. Such a signal can be defined using the signal resulting from the calibration method described above and adjusting the test-generator equalization. If the receiver under test is more capable than the reference (CTLE+DFE) receiver, the receiver under test may not require the transmitter to change its equalization levels to achieve a BER < 10^{-12}. In any case, equalization settings resulting from this procedure must be used for the receiver test and if the receiver requires the transmitter equalization to change, such change must be accommodated by the test set-up used.

A specific methodology for this procedure is outside the scope of this specification. Refer to compliance program test procedures for specific test equipment for specific methodology details.

The 128/130b compliance pattern must be used during eye height and eye width calibration for this test. Modified compliance pattern is used when the receiver test is run.

Table c-d: Long Channel Add-in Card Minimum Receiver Path Sensitivity Requirements at 8.0 GT/s

Parameter	Calibration Target	Unit	Comments
$V_{RX-EH-8G}$ Eye Height	34 (at 10^{-12} BER) 46 (at 10^{-6} BER)	mV	Notes 1, 2, 3, 4, 7
$T_{RX-EH-8G}$ Eye Width	41.25 (at 10^{-12} BER)	ps	Notes 1, 2, 3, 7
Rj (Random Jitter)	3	ps RMS	Notes 5, 6, 7
Sj (Sinusoidal Jitter) 100 MHz	12.5	ps PP	Note 6, 7
Differential Mode Sinusoidal Interference 2.1 GHz	14	mV PP	Note 3,7

Notes:

1. An ideal reference clock without jitter is assumed for this specification.
2. The values in Table c-d are initially calibrated with a reference channel consisting of an 8.0 GT/s M.2 Add-in Card Test Channel followed by 8.0 GT/s M.2 System-Board Test Channel at the transmitter SMP connectors on the System-Board Test Channel. The calibration is done with the same post processing as the System Board 8.0 GT/s transmitter test. After reference calibration, the 8.0 GT/s System-Board Test Channel is removed and the Add-in Card to be tested is placed into the M.2 connector.
3. Eye height and width are specified after the application of the reference receiver. When the optimization of the reference receiver's CTLE and DFE yields an eye height and/or eye width larger than specified, the value for DM-interference is increased.
4. Eye height limits do not account for limitations in test equipment voltage resolution.
5. Rj is applied over the following range. The low frequency limit may be between 1.5 MHz and 10 MHz, and the upper limit is 1.0 GHz. While the nominal value is specified at 3.0 ps RMS, it may be adjusted to meet the value for $T_{RX-EH-8G}$ Eye Width.
6. Rj and Sj are measured without post-processing filters.
7. This is target parameter for Receiver calibration. Allowable tolerances around this nominal number, when doing the calibration are specified in the *PCIe PHY test specification*.

Table e-f: Short Channel Add-in Card Minimum Receiver Path Sensitivity Requirements at 8.0 GT/s

Parameter	Min	Max	Unit	Comments
VRX-EH-8G Eye Height	N/A	N/A	mV	Notes 1, 2, 5
TRX-EH-8G Eye Width	N/A	N/A	ps	Notes 1, 2, 5
Rj (Random Jitter)	3		ps RMS	Note 4
Sj (Sinusoidal Jitter) 100 MHz	12.5		ps PP	
Differential Mode Sinusoidal Interference 2.1 GHz	14		mV PP	Note 3

Notes:

1. An ideal reference clock without jitter is assumed for this specification.

2. The values in Table e-f are initially calibrated with a reference channel consisting of a M.2 Add-in Card short Test Channel followed by M.2 System-Board short Test Channel at the transmitter SMP connectors on the System-Board Short Test Channel. The calibration is done with M.2 compliance test fixtures without any additional ISI board or channel embedding. After reference calibration, the M.2 System-board short Test Channel is removed and the Add-in Card to be tested is placed into a M.2 connector.

3. Eye height and width are specified after application of the reference receiver. When the optimization of the reference receiver's CTLE and DFE yields an eye height and/or eye width larger than specified, the value for DM-interference is increased.

4. Rj is applied over the following range. The low frequency limit may be between 1.5 MHz and 10 MHz, and the upper limit is 1.0 GHz.

5. For the short channel test, the calibrated test equipment transmitter settings from the long channel test are used. Eye height and eye width are not separately re-calibrated.

x.y.3. System Board Transmitter Path Compliance Eye Diagram at 8.0 GT/s

The system board shall pass the eye diagram requirements with at least one of the transmitter equalization presets defined in the PCI Express Base Specification, Chapter 9. The eye diagram requirements are evaluated after the behavioral CDR and the behavioral RX Equalization Algorithm defined in the PCI Express Base Specification, Chapter 9 are applied.

The system board Transmitter path measurements at 8.0 GT/s are made using a two-port measurement methodology. Refer to PCIe CEM specification for the details of the two-port methodology.

All Links are assumed active while generating this eye diagram. The eye diagram requires that the compliance pattern in 128b/130b (refer to the PCI Express Base Specification, Chapter 4) is being transmitted during the test.

Transition and non-transition bits must be distinguished to measure compliance against the de-emphasized voltage level (V_{TXS_d}). V_{TXS} and V_{TXS_d} are minimum differential peak-peak output voltages.

This calculated eye width at BER 10^{-12} must be greater than or equal to T_{TXS}.

The values in Table g-h are referenced to an ideal 100 Ω differential load at the end of an isolated (no crosstalk) test channel consisting of 2.0 inches of 85 Ω trace, followed by a reference receiver package (3.5dB) behind a standard PCI Express edge-finger. This channel shall be referenced as the 8.0 GT/s M.2 System-Board Test Channel. The s-parameters for the channel are provided with this specification. Additional loss from the measurement set-up must be removed. The M.2 System-Board Test Channel is a reference channel for testing and does not represent the worst possible channel that could be implemented on a M.2 compliant Add-in Card.

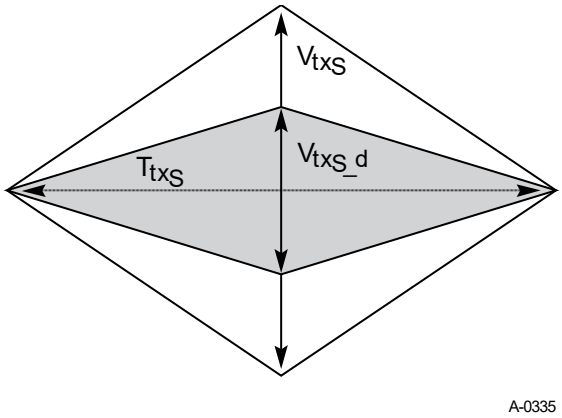
Table g-h: System Board Transmitter Path Compliance Eye Requirements at 8.0 GT/s with Ideal Adaptive TX Equalization

Parameter	Min	Max	Unit	Comments
V_{TXS}	34 (10^{-12} BER) 46 (10^{-6} BER)	1300	mV	
V_{TXS_d}	34 (10^{-12} BER) 46 (10^{-6} BER)	1300	mV	
T_{TXS}	41.25 (10^{-12} BER)		ps	Notes 1

Notes:

1. T_{TXS} is the minimum eye width. The recommended sample size for this measurement is at least $1.5x10^6$ UI.

Figure x: 8.0 GT/s System Board Transmitter Path Composite Compliance Eye Diagram



x.y.4. System Board Minimum Receiver Path Sensitivity Requirements at 8.0 GT/s

The minimum sensitivity values for the system board Receiver path compliance at 8.0 GT/s are defined in Table k-l. The receiver path shall be tested with a worst-case eye to verify that it achieves a BER < 10^{-12}. This worst-case eye is calibrated using transmitter equalization settings that are optimal with the reference equalizer for the calibration channel. After calibration, the test-generator's equalization settings may be adjusted using the transmitter equalization setting in the required transmitter equalization space preferred by the device under test, without changing any other parameter of the test signal or recalibrating the test signal.

If the test generator's transmitter equalization settings are adjusted away from the optimal settings and the test generator is not able to change transmitter equalization without impacting other calibrated parameters – then the other parameters must be adjusted back to the specified values.

If the test is not run in a way that produces the worst-case cross-talk that would be present with all lanes active, the additional cross-talk must be accounted for in some other way.

While the receiver's capacity to adapt its own equalization is part of the test described above, its ability to request the link partner's transmitter to change its equalization settings is tested by applying a signal whose equalization settings are sub-optimal compared to the jitter sensitivity test signal described above. For this signal, the reference receiver would not be able to achieve proper equalization by means of its own CTLE and DFE alone. Such a signal can be defined using the signal resulting from the calibration method described above and adjusting the test-generator equalization. If the receiver under test is more capable than the reference (CTLE+DFE) receiver, the receiver may not require the transmitter to change its equalization levels to achieve a

BER < 10^{-12}. In any case, equalization settings resulting from this procedure shall be used for the above receiver test and, if the receiver requires the transmitter equalization to change, the change accommodates the test set-up used. A specific methodology for this procedure is outside the scope of this specification.

The 128/130b compliance pattern must be used during eye height and eye width calibration for this test. Modified compliance pattern is used when the receiver test is run.

Table k-l: System Board Minimum Receiver Path Sensitivity Requirements at 8.0 GT/s

Parameter	Calibration Target	Max	Unit	Comments
$V_{RX-EH-8G}$ Eye height	34 (at 10^{-12} BER)	34	mV	Notes 1, 2, 3, 4, 7
$T_{RX-EH-8G}$ Eye width	41.25 (at 10^{-12} BER)	41.25	ps	Notes 1, 2, 3, 7
Rj (Random Jitter)	3		ps RMS	Notes 5, 6, 7
Sj (Sinusoidal Jitter) 100 MHz	12.5		ps PP	Note 6, 7
Differential Mode Sinusoidal Interference 2.1 GHz	14		mV PP	Note 3, 7

Notes:

1. The system board reference clock is assumed for this specification. Eye height and width values refer to BER at 10^{-12}.
2. The values in this table are initially calibrated with a reference channel consisting of an 8.0 GT/s M.2 System Board Test Channel followed by 8.0 GT/s M.2 Add-in Card Test Channel at the TX SMP connectors on the M.2 Add-in Card Test Channel. The calibration is done with the same post processing as the M.2 Add-in Card 8.0 GT/s transmitter test. After reference calibration, the 8.0 GT/s M.2 Add-in Card Test Channel is removed, and the M.2 System Board Test Channel is connected to the System Board to be tested.
3. Eye height and width are specified after the application of the reference receiver. When the optimization of the reference receiver's CTLE and DFE yields an eye height and/or eye width larger than specified, the value for DM-interference is increased.
4. Eye height limits do not account for limitations in test equipment voltage resolution.
5. Rj is applied over the following range. The low frequency limit may be between 1.5 and 10 MHz, and the upper limit is 1.0 GHz. While the nominal value is specified at 3.0 ps RMS, it may be adjusted to meet the value for $T_{RX-EH-8G}$ Eye Width.
6. Rj and Sj are measured without post-processing filters.
7. This is target parameter for Receiver calibration. Allowable tolerances around this nominal number, when doing the calibration are specified in the *PCIe PHY test specification*.